WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

an internal circuit receiving supply of an operating current from a power supply node;

a current switch connected between an operating voltage source and said power supply node; and

a leakage detecting circuit for detecting whether a leakage current of said internal circuit is not greater than a reference level,

said leakage detecting circuit including

a reference current supply portion supplying a current of said reference level to said power supply node in an off period of said current switch, and

a voltage comparison circuit for comparing a voltage of said power supply node with a prescribed voltage in said off period.

2. The semiconductor device according to claim 1, wherein said reference current supply portion has a reference current adjust portion which changes said reference level stepwise in response to an adjustment designation.

3. The semiconductor device according to claim 1, further comprising:

an internal voltage control circuit controlling an internal voltage applied to a field effect transistor constituting said internal circuit; and

an internal voltage interconnection transmitting said internal voltage;

said internal voltage control circuit including

an internal voltage comparison circuit comparing a voltage of said internal voltage interconnection with an object voltage,

a voltage control circuit controlling said internal voltage based on a comparison result in said internal voltage comparison circuit, and

a voltage adjust portion for changing said object voltage in response

to an adjustment input.

4. The semiconductor device according to claim 3, wherein said adjustment input being input in a standby mode is set based on a state where said leakage current becomes not greater than said reference level at the time of an operation test.

5. The semiconductor device according to claim 3, wherein
said current switch is turned off in a standby mode, and
said adjustment input to said voltage adjust portion is set based on an output of said voltage comparison circuit.

6. The semiconductor device according to claim 1, wherein said internal circuit includes at least one field effect transistor,
said semiconductor device further comprising:
an internal voltage control circuit for controlling an internal voltage applied to one of source, gate, drain and substrate of said field effect transistor included in said internal circuit; and
an internal voltage interconnection transmitting said internal voltage;
said internal voltage control circuit including
an internal voltage comparison circuit for comparing a voltage of said internal voltage interconnection with an object voltage,
a voltage control circuit controlling said internal voltage based on a comparison result in said internal voltage comparison circuit, and
a voltage adjust portion for changing said object voltage in response to an adjustment input.

7. The semiconductor device according to claim 6, wherein said adjustment input differs in a normal operation mode and a standby mode.

8. The semiconductor device according to claim 6, wherein
said voltage adjust portion includes a voltage-divider circuit which

divides a voltage difference between said internal voltage and a prescribed voltage with a divide ratio in accordance with said adjustment input, and

said internal voltage comparison circuit compares the divided voltage output from said voltage-divider circuit with a fixed reference voltage.

9. A semiconductor memory device, comprising:

a plurality of memory cells each having data written therein in response to supply of a data write current;

a transistor formed of a field effect transistor and driving said data write current;

an internal voltage control circuit controlling an internal voltage applied to said transistor; and

an internal voltage interconnection transmitting said internal voltage;

said internal voltage control circuit including

an internal voltage comparison circuit for comparing a voltage of said internal voltage interconnection with an object voltage,

a voltage control circuit controlling said internal voltage based on a comparison result in said internal voltage comparison circuit, and

a voltage adjust portion for changing said object voltage in response to an adjustment input.

10. The semiconductor memory device according to claim 9, wherein said internal voltage is applied to said transistor as a substrate voltage.

11. The semiconductor memory device according to claim 9, wherein said internal voltage is applied to one of source, gate and drain of said transistor.

12. The semiconductor memory device according to claim 9, further comprising:

a data read circuit for reading data out of said plurality of memory cells; and

a write test portion for evaluating, in an operation test where said adjustment input can be set in a plurality of steps, whether said data of a prescribed level can be written correctly to said plurality of memory cells in each of said plurality of steps;

wherein said adjustment input in a normal operation is set based on the evaluation by said write test portion in said operation test.

13. The semiconductor memory device according to claim 12, wherein

said write test portion includes a data comparison circuit, and

said data comparison circuit compares, in said operation test, data read out of said plurality of memory cells by said data read circuit after writing of data of said prescribed level with data of an expected value corresponding to said prescribed level.

14. The semiconductor memory device according to claim 12, wherein said adjustment input in a standby mode is set different from that in said normal operation.

15. The semiconductor memory device according to claim 9, further comprising:

an access control circuit for switching accesses to said plurality of memory cells based on an input address, between a first mode where each of said plurality of memory cells stores data of one bit and a second mode where each pair of said plurality of memory cells stores data of one bit;

a data read circuit performing data read from at least one of said plurality of memory cells selected as an access target by said access control circuit; and

a data write circuit performing data write to the at least one of said plurality of memory cells selected as said access target.

16. The semiconductor memory device according to claim 9, further comprising a data write circuit controlling said data write current in accordance with a level of said data to be written, wherein

each of said plurality of memory cells includes

a first magnetic layer having a fixed magnetization direction,

a second magnetic layer magnetized in a direction corresponding to a magnetic field generated by said data write current, and

an insulating film formed between said first and second magnetic layers.

17. The semiconductor memory device according to claim 9, further comprising a data write circuit controlling said data write current in accordance with a level of said data to be written, wherein

each of said plurality of memory cells includes

a heating element which generates heat by said data write current, and

a phase change element which is heated by said heating element and makes a transition between two phase states.

18. A semiconductor memory device, comprising:

a plurality of memory cells each having data written therein in response to supply of a data write current;

a first write current line arranged for each of prescribed groups of said plurality of memory cells and having said data write current flown thereon in one of first and second directions;

a plurality of transistors driving said data write current,

said plurality of transistors including

a first driver transistor for driving the current of said first direction to said first write current line, and

a second driver transistor for driving the current of said second direction to said first write current line; and

a first current adjust portion capable of adjusting current amounts flown by said first and second driver transistors independently from each

other.

19. The semiconductor memory device according to claim 18, wherein the direction of said data write current flown on said first write current line is set in accordance with write data.

20. The semiconductor memory device according to claim 18, further comprising a second write current line provided in a direction crossing said first write current line and having said data write current flown thereon in a prescribed direction, wherein

said plurality of transistors further include a third driver transistor for driving the current of said prescribed direction to said second write current line,

said semiconductor memory device further comprising a second current adjust portion adjusting a current amount flown by said third driver transistor.

21. The semiconductor memory device according to claim 20, wherein

said second current adjust portion includes

a plurality of voltage generating circuits respectively generating a plurality of voltages adjustable independently from each other, and

a selector circuit selecting one of said plurality of voltages in accordance with the write data to apply to said third driver transistor, and

said third driver transistor is capable of supplying a current corresponding to the voltage applied via said selector circuit to said second write current line.

22. The semiconductor memory device according to claim 18, further comprising:

a second write current line provided in a direction crossing said first write current line and having said data write current flown thereon in a prescribed direction; and

a second current adjust portion supplying one of first and second current amounts to said second write current line,

said second current adjust portion including

a first current supply portion supplying a current corresponding to an adjustable first reference voltage,

a second current supply portion supplying a current corresponding to an adjustable second reference voltage, and

a switch element arranged such that one of the current supplied from said first current supply portion and a sum or difference of the currents supplied from said first and second current supply portions is selectively supplied to said second write current line in accordance with on/off control of said switch element,

said first reference voltage being adjusted corresponding to one of said first and second current amounts, and

said second reference voltage being adjusted corresponding to a difference between said first and second current amounts.

23. The semiconductor memory device according to claim 22, wherein on/off of said switch element is controlled in accordance with the write data.

24. The semiconductor memory device according to claim 18, wherein said first current adjust portion includes a voltage generating circuit generating first and second voltages adjustable independently from each other,

said semiconductor memory device further comprising a connection switching circuit provided between said voltage generating circuit and said first and second driver transistors,

said connection switching circuit being capable of switching between a first connection for applying said first and second voltages to said first and second driver transistors, respectively, and a second connection for applying said second and first voltages to said first and second driver transistors, respectively, for each access to said semiconductor memory device, and

said first and second driver transistors being capable of supplying to said first write current line a current amount corresponding to a voltage applied via said connection switching circuit.

25. The semiconductor memory device according to claim 18, wherein said plurality of memory cells each have an asymmetrical shape so that said data write current necessary for data write differs in magnitude in accordance with an arranged direction of the memory cell.

26. The semiconductor memory device according to claim 25, wherein said first current adjust portion includes a voltage generating circuit generating first and second voltages adjustable independently from each other,

said semiconductor memory device further comprising a selector circuit provided between said voltage generating circuit and said first and second driver transistors and switching which of said first and second voltages is applied to respective one of said first and second driver transistors for each access to said semiconductor memory device,

said first and second driver transistors each being capable of supplying a current corresponding to the voltage applied via said selector circuit to said first write current line.

27. The semiconductor memory device according to claim 26, wherein said selector circuit switches which of said first and second voltages is applied to respective one of said first and second driver transistors in accordance with information capable of identifying said arranged direction of the memory cell selected as a target of said data write from among said plurality of memory cells.

28. The semiconductor memory device according to claim 18, wherein

said plurality of memory cells each have an asymmetrical shape so that said data write current necessary for data write differs in magnitude in

accordance with an arranged direction of the memory cell, and

in each of said plurality of memory cells, the magnitude of said data write current necessary for the data write differs between said first and second directions.

29. The semiconductor memory device according to claim 28, wherein said first current adjust portion includes a voltage generating circuit generating first and second voltages adjustable independently from each other,

said semiconductor memory device further comprising a connection switching circuit provided between said voltage generating circuit and said first and second driver transistors,

said connection switching circuit being capable of switching between a first connection for applying said first and second voltages to said first and second driver transistors, respectively, and a second connection for applying said second and first voltages to said first and second driver transistors, respectively, for each access to said semiconductor memory device, and

said first and second driver transistors each being capable of supplying a current amount corresponding to the voltage applied via said connection switching circuit to said first write current line.

30. The semiconductor memory device according to claim 29, wherein said connection switching circuit switches between said first and second connections in accordance with information capable of identifying said arranged direction of the memory cell selected as a target of said data write from among said plurality of memory cells.

31. The semiconductor memory device according to claim 18, further comprising a plurality of second write current lines provided in a direction crossing said first write current line and each having said data write current flown thereon in a prescribed direction irrelevant to said write data, wherein

said plurality of transistors further include a plurality of third driver

transistors provided corresponding to said plurality of second write current lines and each driving a current in a fixed direction as seen from itself to corresponding said second write current line,

said plurality of third driver transistors are arranged alternately on one end side and on another end side of said plurality of second write current lines for every said second write current line,

said first current adjust portion includes a voltage generating circuit generating first and second voltages adjustable independently from each other,

said first driver transistor is capable of supplying to said first write current line a current amount corresponding to one of said first and second voltages that is selected in accordance with address information capable of identifying whether said third driver transistor corresponding to a data write target is arranged on said one end side or on said another end side, and

said second driver transistor is capable of supplying to said first write current line a current amount corresponding to the other of said first and second voltages that is complementarily selected in accordance with said address information.